

Appl. No. 10/596,216
Amdt. Dated June 12, 2007
Reply to Office Action of March 21, 2007

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REMARKS

Claims 1 to 10 are currently pending in the present application. Claims 1 to 4, 6 and 8 stand rejected by the Action under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,886,353 to Spivey et al. (hereinafter "Spivey"). Applicants respectfully submit that Spivey does not expressly or inherently disclose all of the elements set forth in independent claim 1. Thus, Spivey does not anticipate claim 1 or claims 1 to 9, which depend therefrom.

Claim 1 claims a detector for an imaging device, comprising a substrate; an array of sensor elements, which is formed on one side of the substrate; at least one integrated electronic module for processing sensor signals, the module being mounted at one edge of the substrate and being connected at its input side to the sensor elements, and the module comprising at least one analog-digital converter for conversion of analog input signals into digital output signals.

Spivey fails to disclose the invention of claim 1. Specifically, Spivey fails to disclose an array of sensor elements, which is formed on one side of the substrate. Rather, as discussed at column 4, lines 2 to 5, Spivey merely discloses an electronic readout array which is "fabricated on and in the upper surface of a substrate". As illustrated in Fig. 1, the array is at least disposed along two sides of the substrate. Thus, Spivey does not disclose an array of sensor elements, which is formed on one side of the substrate.

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Spivey also fails to disclose at least one integrated electronic module for processing sensor signals, the module being mounted at one edge of the substrate. The term "mounted" is defined by the subject application as mechanically fixed, at one edge of the substrate. Fig. 1 of the subject application clearly shows that the electronic module is an integral component of the imaging device, being mounted to the substrate. In contrast, as illustrated in Fig. 1, the electronic readout array of Spivey is a separate and distinct element that is connected to a substrate by an additional element such as a wire lead. As discussed in Spivey, "[w]ire bond pads 33 at the periphery of the electronic readout array 12 connect the readout circuit 18 to data acquisition electronics 20 as shown in FIG. 1" (Column 5, lines 1 to 3). Thus, Spivey clearly does not disclose an electronic module that is mounted to the substrate.

The above described features claimed in claim 1 and not disclosed by Spivey enable the detector of the present invention to achieve analog-digital conversion of the sensor element signals directly at the edge of the array of sensor elements, thereby avoiding signal interference and noise caused by long external leads, such as those disclosed by Spivey. Further advantages provided by the integrated module of claim 1 being fixedly connected to the substrate include a mechanically robust design and optimization both of the array of sensor elements and of the integrated module. Moreover, higher overall yield and reduction in costs can be achieved in manufacture of the detector of claim 1.

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Dependent claims 2 to 4, 6 and 8 depend from claim 1 and provide further features, thus claims 2 to 4, 6 and 8 are clearly distinguishable over Spivey for at least the reasons discussed. Accordingly, the Applicants respectfully request that the rejections under 35 U.S.C. § 102(e) of claims 1 to 4, 6 and 8 be withdrawn.

Claims 1 to 4 and 9 and 10 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,403,964 to Kyyhjynen (hereinafter "Kyyhjynen"). Kyyhjynen, similar to Spivey, fails to disclose an array of sensor elements, which is formed on one side of the substrate, as clearly claimed in claim 1. In contrast, as discussed in Kyyhjynen at column 8, lines 37 to 45 and as illustrated in Fig. 4, an imaging device called a tile 90 is tilted by means of a wedge 80 or an equivalent structure. In this manner, an active region 94 of a tile (say 90.1) covers an inactive region 92 of a subsequent tile (i.e. the adjacent tile 90.2). This tiling scheme fails to anticipate an array of sensor elements, which is formed on one side of the substrate, as claimed in claim 1.

Dependent claims 2 to 4, 9 and 10 depend from claim 1 and provide further features, thus claims 2 to 4, 9 and 10 are clearly distinguishable over Kyyhjynen for at least the reasons discussed. Accordingly, the Applicants respectfully request that the rejections under 35 U.S.C. § 102(e) of claims 1 to 4, 9 and 10 be withdrawn.

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Claim 7 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Kyyhjynen. Applicants respectfully submit that claim 7, depending from claim 1, is patentable over Kyyhjynen for at least the reason that Kyyhjynen fails to teach or suggest all the claim limitations of claim 1, as discussed. Specifically, Kyyhjynen fails to disclose an array of sensor elements, which is formed on one side of the substrate. Claim 7 further claims that the integrated module is connected to the substrate by flip-chip contacting, by wire-bonding or by mounting of packaged ICs on a wafer. As conceded by the Action, Kyyhjynen does not disclose a method for mounting the processing chips onto the substrate, thus Kyyhjynen clearly fails to disclose the invention of claim 7, which depends from claim 1.

Claims 5 and 8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kyyhjynen in view of Spivey. Applicants respectfully submit that claims 5 and 8, depending from claim 1 are patentable over both Kyyhjynen and Spivey because both Kyyhjynen and Spivey, taken either alone or in combination fail to teach or suggest all the claim limitations of claim 1, as discussed. Specifically, the cited combination fails to disclose an array of sensor elements, which is formed on one side of the substrate. Claim 5 further claims that the integrated module is manufactured from crystalline silicon. Claim 8 further claims that the substrate comprises electronics of crystalline or amorphous silicon. Applicants respectfully assert that neither claim 5 nor 8 are rendered obvious by the cited combination.

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Allowance of claims 1 to 10 is earnestly solicited.

Conclusion

In view of the foregoing, Applicants respectfully submit that the specification, the drawings and all claims presented in this application are currently in condition for allowance. Accordingly, Applicants respectfully request favorable consideration and that this application be passed to allowance.

Should any changes to the claims and/or specification be deemed necessary to place the application in condition for allowance, the Examiner is respectfully requested to contact the undersigned to discuss the same.

Applicants' representative believes that this response is being filed in a timely manner. In the event that any extension and/or fee is required for the entry of this amendment the Commissioner is hereby authorized to charge said fee to Deposit Account No. 14-1270. An early and favorable action on the merits is earnestly solicited.

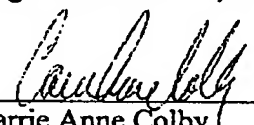
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If the Examiner should have any questions concerning this communication or feels that an interview would be helpful, the Examiner is requested to call David Barnes, Esq., Intellectual Property Counsel, Philips North America Corporation at the number below.

Respectfully submitted,

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